QUERY CONTROL FORM

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Application No.	09/832,685	Prepared by	Lois Stone	Tracking Number	5926800
Examiner-GAU	Chang – 2819	Date	7/20/04	Week Date	3/29/04
		No. of queries	1	ZFW	

JACKET

a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing

b. Text Continuity

c. Holes through Data

d. Other Missing Text

e. Illegible Text

f. Duplicate Text

g. Brief Description

h. Sequence Listing

i. Appendix

j. Amendments

k. Other

CLAIMS

a. Claim(s) Missing

b. Improper Dependency

c. Duplicate Numbers

d. Incorrect Numbering

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g. Amendments

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k. Other

MESSAGE

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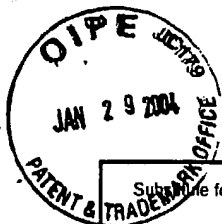
Thank you,

initials

RESPONSE

initials

E-5 (Rev. 10/01/02)

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

| Sheet | 1 | of | |

Complete if Known	
Application Number	09/832,685
Filing Date	April 10, 2001
First Named Inventor	Reddy, Srinivas
Art Unit	2819
Examiner Name	Daniel D. Chang
Attorney Docket Number	015114-045720US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number — Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	0001	US-4609986	09-02-1986	Hartmann et al.	
	0002	US-4617479	10-14-1986	Hartmann et al.	
	0003	US-4677318	06-30-1987	Veenstra et al.	
	0004	US-4713792	12-15-1987	Hartmann et al.	
	0005	US-4871930	10-03-1989	Wong et al.	
	0006	US-4899067	02-06-1990	So et al.	
	0007	US-4912342	03-27-1990	Wong et al.	
	0008	US-5121006	06-09-1992	Pedersen et al.	
	0009	US-5144166	09-01-1992	Camarota et al.	
	0010	US-5185706	02-09-1993	Agrawal et al.	
	0011	US-5208491	05-04-1993	Ebeling et al.	
	0012	US-5241224	08-31-1993	Pedersen et al.	
	0013	US-5260610	11-09-1993	Pedersen et al.	
	0014	US-5260611	11-09-1993	Cliff et al.	
	0015	US-5268598	12-07-1993	Pedersen	
	0016	US-5329180	06-12-1994	Popli et al.	
	0017	US-5343406	08-30-1994	Freeman et al.	
	0018	US-5350954	09-27-1994	Patel et al.	
	0019	US-5355035	10-11-1994	Vora et al.	
	0020	US-5406133	04-11-1995	Vora et al.	
	0021	US-5444394	08-22-1995	Watson et al.	
	0022	US-5497108	03-05-1996	Menon et al.	
	0023	US-5504440	04-02-1996	Sasaki	
	0024	US-5506517	04-09-1996	Tsui et al.	
	0025	US-5548229	08-20-1996	Segawa et al.	
	0026	US-5581199	12-03-1996	Pierce et al.	
	0027	US-5614840	03-25-1997	McClintock et al.	
	0028	US-5614844	03-25-1997	Sasaki et al.	
	0029	US-5652904	07-29-1997	Trimberger	
	0030	US-5705938	01-06-1998	Kean	
	0031	US-6002268	12-14-1999	Sasaki et al.	
	0032	US-6025735	02-15-2000	Vora et al.	

FOREIGN PATENT DOCUMENTS

Examiner	Cite	Foreign Patent Document	Publication Date	Name of Patentee or	Pages, Columns, Lines,	T[6]

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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	Complete if Known	
Application Number	09/832,685	
Filing Date	April 10, 2001	
First Named Inventor	Reddy, Srinivas	
Art Unit	2819	
Examiner Name	Daniel D. Chang	

Sheet	2	of		Attorney Docket Number	015114-045720US

		Country Code[3] Number[4] Kind Code[5] *(if known)*				
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Examiner Signature		Date Considered	

PTO/SB/08B (08-03)

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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			Complete if Known
	Application Number		09/832,685
	Filing Date		April 10, 2001
	First Named Inventor		Reddy, Srinivas
	Art Unit		2819
	Examiner Name		Daniel D. Chang
Sheet	3	of	Attorney Docket Number	015114-045720US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	0033	Scarpero, Jr., Field-Effect Transistor Bidirectional Driver Control Circuit, IBM TDB, vol. 16, No. 8, pp. 2442-2443, Jan. 1974.	
	0034	Rhyne, Fundamentals of Digital Systems Design, N. J., pp 70-71, 1973.	
	0035	Anonymous, Tri-State Double inverter Buffer, Research Disclosure, p. 30511, Sep. 1989.	
	0036	Xilinx Corp., The Programmable Logic Data Book, "XC4000, XC4000A, XC4000H, Logic Cell Array Families," pp. 2-7 to 2-46 (1994).	
	0037	Xilinx Corp., The Programmable Logic Data Book, "XC3000, XC3000A, XC3000L, XC3100, XC3100A, Logic Cell Array Families," pp. 2-105 to 2-124 (1994).	
	0038	Xilinx Corp., The Programmable Logic Data Book, "XC3000, XC3000A, XC3000L, XC3100, XC3100A, Logic Cell Array Families," pp. 2-105 to 2-152 (1994).	
	0039	Altera Data Book, Altera Classic, Programmable Logic Device Family, pp. 235-244, 08/93.	
	0040	Altera Data Book, Max 5000 Programmable Logic Device Family, pp. 149-160, 08/93.	
	0041	Altera Data Book, Max 7000 Programmable Logic Cell Device Family, pp. 69-81, 08/93.	
	0042	Altera Data Book, Flex 8000 Programmable Logic Device Family, pp. 29-47, 08/93.	
	0043	Altera Data Book, Introduction, pp. 3-16, 08/93.	

Examiner Signature		Date Considered	

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